## REMARKS

The Applicant does not believe that examination of the foregoing amendment will result in the introduction of new matter into the present application for invention. Therefore, the Applicant, respectfully, requests that the above amendment be entered in and that the claims to the present application, kindly, be reconsidered.

The Office Action dated March 24, 2005 has been received and considered by the Applicant. Claims 1-7 are pending in the present application for invention. Claims 1-7 are rejected by the March 24, 2005 Office Action. The foregoing amendment to Claims 1-6 has eliminated reference numerals; which should not be seen as a narrowing amendment. Therefore, the amendment to Claims 1-6 should not restrict the application of the Doctrine of Equivalents to these claims.

The Examiner takes **Official Notice** that it is notoriously well known in the art to use multiple memory blocks with an arbitrator using indicators and addresses to increase the speed and efficiency of the memory. The Applicant respectfully points out that subject matter defined by the rejected claims is for the multi-processor unit to include blocks of electronic memory and the communication means includes block-based communication means connected to the memory blocks and connected to one or more of the first domain processors and one or more of the second domain processors for selectively interconnecting the connected processors to the memory blocks, with only one processor at a time being interconnected to one of the memory blocks, and processors of different domains being interconnected at different times to the same memory block. This subject matter is not disclosed or suggested by the prior art. The Applicant, respectfully requests that the Examiner provide prior art references illustrating memory structures used in a manner as defined by the rejected claims.

The Applicant respectfully points out that the rejected claims additionally define subject matter for an electronic memory; block-based communication means connected to the memory blocks to provide access to the memory blocks; stream-based communication means; a plurality of processors connected to the block-based communication means for processing data in the memory blocks and connected to the stream-based communication means for providing data objects from a processor to a subsequent processor, the data objects including data for processing the data and pointers

to memory blocks to control access to the memory blocks, the processors having means for data flow driven process control so that receiving data objects from a previous processor through the stream-based communication means triggers processing by the subsequent processor that receives those data objects, each processor having exclusive control for accessing data in one or more of the memory blocks, and each processor receiving the exclusive control of a memory block by receiving the pointer to the memory block from the previous processor through the stream-based communications means and each processor yielding exclusive control to the subsequent processor by providing a pointer to the memory block to the subsequent processor through the stream-based communication means. This subject matter is not disclosed or suggested by the prior art. The Applicant, respectfully requests that the Examiner provide prior art references illustrating memory structures used in a manner as defined by the rejected claims.

The Examiner takes **Official Notice** that it is notoriously well known in the art to use a periodic sequencer so as to require less circuitry, thereby reducing cost and power consumption. The Applicant, respectfully points out that the rejected claims define subject matter for at least one of the domain control processors includes a periodic sequencer that initiates control commands transmitted to other processors to initiate subroutines in those processors depending on an index counter. The Applicant, respectfully, asserts that this subject matter is not disclosed or suggested by the prior art. The Applicant requests that the Examiner provide prior art references illustrating a periodic sequencer that initiates control commands transmitted to other processors to initiate subroutines in those processors depending on an index counter as defined by rejected claims.

The Examiner takes **Official Notice** that it is notoriously well known in the art of signal processing techniques, such as FFT, IFFT, equalization, and forward error correction to transform the signal from one type to another. The Applicant, respectfully points out that the rejected claims define subject matter for processing of the first domain including FFT and IFFT processing of blocks of data in the memory blocks, with the processing of the second domain including equalization of blocks of data in the memory blocks. The Applicant, respectfully, asserts that this subject matter is not disclosed or suggested by the prior art. The Applicant requests that the Examiner provide prior art

references illustrating processing of the first domain including FFT and IFFT processing of blocks of data in the memory blocks with the processing of the second domain including equalization of blocks of data in the memory blocks as defined by the rejected claims.

Claim 1-7 are rejected as being obvious in view of numerous prior art references as described below. The MPEP at §2143 states that to "establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

Claims 1-2 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,502,512 issued in the name of Toyoda et al. (hereinafter referred to as Toyoda et al.) in view of US Patent No 6,081,783 issued in the names of Divine et al. (hereinafter referred to as Divine et al.).

Regarding Claim 1, the rejection asserts that Toyoda et al. disclose an apparatus and method for digital video and audio processing with information input and output processing devices. The rejection reads the subject matter for a "first domain processing means for first processing data depending on first domain configuration information" broadly and asserts that this subject matter is taught by Toyoda et al. The Examiner states that in Col 2, lines 49-52 as well as numerals 101, 102, and 103 in FIG. 1 of Toyoda et al. are information input and output processing means for entering video or audio information, and putting out directly or after arithmetic processing of video or audio information". The Applicant, respectfully, asserts that Toyoda et al. do not disclose, or suggest, first domain processing means for first processing data depending on first domain configuration information.

The Examiner states item 102 in Fig. 1 teaches the subject matter for a "second domain processing means (110) for second processing the first processed data depending second domain configuration information, the second processing being different than the first processing". The Examiner's position is that the statement for second processing means are different than the first processing in that Toyoda et al, at Col 4, lines 31-34 discloses that the process to be executed by the "domains' is controlled by the control means 105. The Applicant does not concur with this assertion. Toyoda et al. do not disclose, or suggest, the subject matter for the second domain processing means second processing the first processed data depending on the configuration of the second domain information with the second processing being different than the first processing.

The Examiner further states that the subject matter of "a global control processor (120) connected to the communication means for providing the first domain configuration information and the second domain configuration information through the configuring first and second domains" is met by Control means 105. The Applicant does not concur with this assertion. Toyoda et al. do not disclose, or suggest, a global control processor (120) connected to the communication means for providing the first domain configuration information and the second domain configuration information through the configuring first and second domains.

The rejection admits that Toyoda et al. fail to disclose the concept the first and second "domains" having multiple processors as defined by the rejected claims. The rejection contends that Divine et al. teach the concept of using multiple processors in a particular "domain' so as to improve the overall speed and efficiency.

The Applicant, respectfully, points out that rejected Claim 1 defines subject matter for the first domain processors including a first domain control processor (105) for controlling the first processing of the first domain and the second domain processors including a second domain control processor (111) for controlling the second processing of the second domain. It should be noted that there is no mention of the first domain control processor or the second domain control processor within the rejection. Therefore, all the subject matter defined by rejected Claim 1 is not found in the combination made by the rejection.

The Applicant, respectfully, points out that rejected Claim 1 defines subject matter for each first domain processor differently sub-processing the data in order to first process the data. It should be noted that there is no mention of each second domain processor differently sub-processing the data in order to second process the data within the rejection. Therefore, all the subject matter defined by rejected Claim 1 is not found in the combination made by the rejection.

The Applicant, respectfully, points out that rejected Claim 1 defines subject matter for each second domain processor differently sub-processing the data in order to second process the data. It should be noted that there is no mention of each second domain processor differently sub-processing the data in order to second process the data within the rejection. Therefore, all the subject matter defined by rejected Claim 1 is not found in the combination made by the rejection.

For the foregoing reasons, this rejection is, respectfully, traversed.

Regarding claims 2 and 7, the rejection asserts that claimed limitations of "the communication means include a stream-based communication means (101) connected to the global control processor and connected to a plurality of the processors of the first and second domains including the first and second domain control processors for transmitting information streams between connected processors" and "the stream-based communications means are connected to an input/output bus (120) to at times receive stream of data into the multi-processor unit through the stream-based communications means in to one of the connected processors and to at other times transmit a stream of data from one of the connected processors through the stream-based communications means onto the input/output bus" are met by the bus means 107 of Figure 1. The Applicant does not concur with this assertion. Toyoda et al. do not disclose, or suggest, the subject matter for the communication means include a stream-based communication means connected to the global control processor and connected to a plurality of the processors of the first and second domains including the first and second domain control processors for transmitting information streams between connected processors.

The rejection alleges that the combination of Toyoda et al. with Divine et al. explicitly and implicitly discloses the use of memory. The Examiner admits that the

combination fails to disclose blocks of memory with selective interconnections to the plurality of processors. The rejection takes Official Notice that it is notoriously well known in the art to use multiple memory blocks with an arbitrator using indicator and addresses so as to increase the speed and efficiency of the memory and therefore obvious to one of ordinary skill in the art to the aforementioned combination with multiple memory blocks with an arbitrator using indicator and addresses so as to increase the speed and efficiency of the memory. The Applicant respectfully points out that subject matter defined in Claim 2 is for the multi-processor unit to include blocks of electronic memory and the communication means includes block-based communication means connected to the memory blocks and connected to one or more of the first domain processors and one or more of the second domain processors for selectively interconnecting the connected processors to the memory blocks, with only one processor at a time being interconnected to one of the memory blocks, and processors of different domains being interconnected at different times to the same memory block. This subject matter is not disclosed or suggested by the prior art. The Applicant, respectfully requests that the Examiner provide prior art references illustrating memory structures used in a manner as defined by Claim 2. The Applicant, respectfully requests that the Examiner provide prior art references illustrating memory structures used in a manner as defined by Claim 2.

The rejection alleges that the subject matter for control of the domain control processors during operation includes data flow control so that receiving a data object through the stream-based communication means triggers processing by the domain control processor" is met by items 105 and 107 of Figure 1. The Applicant, respectfully, disagrees. The subject matter for triggering processing by the domain control processor upon receiving a data object through the stream-based communication means is not disclosed or suggested by the combination of Toyoda et al. with Divine et al.

The rejection admits that the combined teaching of Toyoda et al. with Divine et al. fails to disclose the use of a periodic sequencer. The rejection takes Official Notice that it is notoriously well know in the art to use a periodic sequencer to require less circuitry, thus reducing cost and power consumption. The Applicant, respectfully points out that Claim 2 defines subject matter for at least one of the domain control processors

includes a periodic sequencer that initiates control commands transmitted to other processors to initiate subroutines in those processors depending on an index counter. The Applicant, respectfully, asserts that this subject matter is not disclosed or suggested by the prior art. The Applicant requests that the Examiner provide prior art references illustrating a periodic sequencer that initiates control commands transmitted to other processors to initiate subroutines in those processors depending on an index counter as defined by Claim 2.

The rejection admits that the combined teaching of Toyoda et al. with Divine et al. fails to disclose that the processing includes FFT, IFFT, equalization, or forward error correction. The Examiner takes **Official Notice** that it is notoriously well known in the art of signal processing techniques, such as FFT, IFFT, equalization, or forward error correction so are to transform (he signal from one type to another. The Applicant, respectfully points out that Claim 2 defines subject matter for processing of the first domain including FFT and IFFT processing of blocks of data in the memory blocks, with the processing of the second domain including equalization of blocks of data in the memory blocks. The Applicant, respectfully, asserts that this subject matter is not disclosed or suggested by the prior art. The Applicant requests that the Examiner provide prior art references illustrating processing of the first domain including FFT and IFFT processing of blocks of data in the memory blocks with the processing of the second domain including equalization of blocks of data in the memory blocks as defined by Claim 2.

The rejection admits that the combined teaching of Toyoda et al. with Divine et al. fails to disclose that the system can decode an 8-VSB signal based on the ATSC standard or decode a COFOM transmission based on the DVB-T standard. The Examiner's position is that it would have been clearly obvious to one of ordinary skill in the art to implement the aforementioned combined teaching with means to decode an 8-VSB signal based on the ATSC standard or decode a COFDM transmission based on the DVB-T standard so as to enable interoperability. The Applicant, respectfully, submits that all the elements defined by the claims must be addressed in order to create a *prima facie* case of obviousness. If the Examiner desires to take Official Notice then it must be

stated that Office Notice is being taken. Otherwise some valid rationale for "obviousness" must be employed.

In view of the aforesaid reasons and arguments, this rejection is traversed.

Claims 3-6 are rejected under 35 U. S. C. 103(a) as being unpatentable over Toyoda et al. in view of Divine et al. and further in view of Integrated Circuits and Microprocessors by R.C. Holland. Claims 3-6 depend from claims that have been previously discussed and are believed to be allowable and further narrow and define these claims. Therefore, Claims 3-6 are also believed to be allowable.

New Claim 8-20 have been added by the foregoing amendment to the claims. New Claims 8-20 generally have a scope similar to elements contained within Claim 2 as originally filed. Therefore, the entry of new Claims 8-20 will not result in the introduction of new matter into the present application for invention. New Claims 8-20 are believed to be allowable because the prior art does not disclose or suggest the subject matter defined by these claims. This subject matter has bee previously discussed in the response top the rejection of Claim 2, *supra*.

Applicant is not aware of any additional patents, publications, or other information not previously submitted to the Patent and Trademark Office which would be required under 37 C.F.R. 1.99.

In view of the foregoing amendment and remarks, the Applicant believes that the present application is in condition for allowance, with such allowance being, respectfully, requested.

Respectfully submitted,

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